Pokhara University

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| Level: Bachelor | Semester: Spring | Year : 2014 |
| Programme: BE | | Full Marks: 100 |
| Course: Computer Organization and Architecture | | Pass Marks: 45 |
| Time : 3hrs. |

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| *Candidates are required to give their answers in their own words as far as practicable.* |
| *The figures in the margin indicate full marks.* |
| Attempt all the questions. |

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|  | 1. Explain the basic computer and CPU organization with the help of block diagram. 2. Describe the assembly process for assembly-language programs. How does it differ from the compilation process?   **OR**  What do you mean by Instruction Set Architecture? What are the major issues to be considered while designing an Instruction Set Architecture? | 7  8 |
|  | 1. Differentiate with suitable example(**any one**): 2. Linear and multiple dimensional organizations of chips. 3. Higher order interleaving and lower order interleaving. 4. What is RTL? Write the RTL for shift operations. Design a 4-bit circular right shifting circuit. | 7  8 |
|  | 1. What are the different topologies used to interconnect MIMD computers? Describe with suitable diagrams. 2. For a very simple CPU with the following instruction sets:  |  |  |  | | --- | --- | --- | | Instruction | Operation | Instruction code | | ADD AAAAAA | AC🡨AC+M[AAAAAA] | 00AAAAAA | | AND AAAAAA | AC🡨AC∧M[AAAAAA] | 01AAAAAA | | COM | AC🡨AC` | 10XXXXXX | | OR AAAAAA | AC🡨ACVM[AAAAAA] | 11AAAAAA |  1. Describe specifications and draw State diagram. 2. Design ALU and Register set. | 5  10 |
|  | 1. Differentiate between Segmentation and Paging? Describe the four most common replacement algorithms related to design issues of cache memory? 2. Explain the generation of micro-operation using horizontal as well as vertical microcode. Write two ways to reduce number of micro-instruction. | 8  7 |
|  | 1. Write the RTL code for the booth's Algorithm. Using the same code to trace the multiplication of (-5) and (4). 2. What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Also describe what the solutions to correct those conflicts are. | 7  8 |
|  | 1. Differentiate Serial and Parallel Communication? Describe 4 different modes of asynchronous data transfer. 2. What is memory hierarchy? Explain the importance of cache memory and virtual memory in the hierarchy. | 7  8 |
|  | Write short notes on: (**Any two**)   1. DMA. 2. Cache Coherence. 3. Instruction Formats. | 2×5 |